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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/088,674	06/02/1998	DANIEL J. MORGAN	TI-25995	2025

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EXAMINER
NGUYEN, KEVIN M

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 02/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/088,674	MORGAN ET AL.	
	Examiner	Art Unit	
	Kevin M. Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The response filed on 12/18/2002 is entered. The rejection of claims 1-10 are maintained.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Barbier et al (US 5,053,764).

As to claim 1, Barbier et al teaches a method of displaying digital image which includes a luminance state presenting a first interval 1/Fo around a mean value b+ (first offset value) and a second interval 1/Fo around a mean value b- (second offset value, col. 5, lines 9-12), the two different binary states of luminance a and b, a is the luminance level of a lit pixel (a first offset pixel value display frame), and b is the luminance level of an off pixel (the opposite/second offset pixel value display frame), the making of the semi-luminance (a+b)/2 (average of a displayed first offset pixel value and a second offset pixel value, figure 3 and 4, col. 5, lines 36-40).

As to claim 2, Barbier et al teaches a luminance state presenting a first interval 1/FO around a mean value b+ (first predetermined amount, col. 5, lines 10-11).

As to claim 3, Barbier et al teaches a luminance state presenting a first interval 1/FO around a mean value b+ (first offset value b+ is greater than a first pixel value b, col. 5, lines 9-12).

As to claim 4, Barbier et al teaches the pixels value a and b extracting from a plurality of weight-bit plane A1, A2 and B1,B2 (col. 3, lines 52-59).

As to claim 5, Barbier et al teaches two pairs of planes A1, B1 and A2, B2 using alternately for reading and writing (a first display frame and a second display frame are consecutive, col. 4, line 65 to col. 5, line 1).

As to claim 6, Barbier et al teaches a system of displaying digital image which includes a graphic processor 2 (logic circuit) controlling/offsetting by a processor 1 (figure 1, col. 3, lines 1-3), a luminance state presenting a first interval 1/Fo around a mean value b+ (first offset value) and a second interval 1/Fo around a mean value b- (second offset value, col. 5, lines 9-12), a display screen 11 (col. 3, lines 4-6) displays the two different binary states of luminance a and b, a is the luminance level of a lit pixel (a first offset pixel value display frame), and b is the luminance level of an off pixel (the opposite/second offset pixel value display frame), the making of the semi-luminance (a+b)/2 (average of a displayed first offset pixel value and a second offset pixel value, figure 3 and 4, col. 5, lines 36-40).

As to claim 7, Barbier et al teaches a graphic processor 2 controlling a luminance state presenting a first interval 1/FO around a mean value b+ (first predetermined amount, col. 5, lines 10-11).

As to claim 8, Barbier et al teaches a graphic processor 2 controlling a luminance state presenting a first interval 1/FO around a mean value b+ (first offset value b+ is greater than a first pixel value b, col. 5, lines 9-12).

As to claim 9, Barbier et al teaches a graphic processor 2 controlling the pixels value a and b extracting from a plurality of weight-bit plane A1, A2 and B1,B2 (col. 3, lines 52-59).

As to claim 10, Barbier et al teaches a graphic processor 3 controlling two pairs of planes A1, B1 and A2, B2 using alternately for reading and writing (a first display frame and a second display frame are consecutive, col. 4, line 65 to col. 5, line 1).

Response to Arguments

4. Applicant's arguments filed 12/18/2002 have been fully considered but they are not persuasive.

In response to applicant's argument that claim 1 recites "offsetting a first pixel value a first predetermined amount to form a first offset pixel value and displaying said first offset pixel value during a first display frame; and offsetting said first pixel value by the opposite of said first predetermined amount to form a second offset pixel value and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value." This argument is not persuasive because the explanation of claim 1 as stated above, Barbier et al's invention further teach at column 5, lines 36-49 "the frame rate control as shown in figures 12A, and 12B, the luminance level of a lit pixel "[+/-] a" = "[+/-] 2" (for example a=2) corresponds to the offsetting value as claimed; a

first offset pixel value a_{RGB} =14 and a second offset pixel value b_{RGB} = 18 (for example a_{RGB} =14 and b_{RGB} = 18 are displaying said first offset pixel value during a first display frame and displaying said second offset pixel value during a second display frame as claimed, see figures 7 and 8); based on the teaching of Barbier et al the four luminance levels a+, a-, b+, b- are averaged during the periods 4/Fo (column 5, lines 43-44); therefore, [+/-] 16 = (14+18) / 2 corresponding to the claimed average of said displayed first offset pixel value and said second offset pixel value is said first pixel value. These arguments are not persuasive because although Barbier et al does not teach the method of offsetting, but before performing the display, the adjacent pixel values have to offset inherently two different frames by the frame rate controlling of a graphic processor 2 (see figures 1, 3, 4, 12A and 12B, column 3, lines 34-50).

In response to applicant's argument that claim 6 recites "a logic circuit offsetting a first pixel value a first predetermined amount to form a first offset value, said logic circuit also offsetting said first said pixel value by the opposite of said first predetermined amount to form a second offset pixel value." This argument is not persuasive because Barbier et al's invention teach a system of displaying digital image which includes a graphic processor 2 (logic circuit) controlling by a processor 1 (figure 1, col. 3, lines 1-3), a graphic processor 2 provides inherently a logic circuit offsetting a first bit a_{jk} stored in electrical form in a first memory plane A and a second bit b_{jk} stored in the second memory plane B (see figure 1, column 3, lines 11-16);

the addressing sequences are performed by the circuit 7 in addressing, for the even-order addressing stages, pixels of the same row and column parity such as ajk

through the plane A, and pixels of opposite row and column parity such as bj,k+1 or bj,k-1 or bj+1,k or bj-1,k through the plane B. For the odd-order addressing stages, the addressing is done for pixels of the same parity by the plane B and for pixels of opposite parity by the plane A, namely, in reverse to what is shown in figure 4 (column 4, lines 3-12);

hatched lines are used to distinguish the pixels corresponding to the luminance information b extracted from the plane B, the non-hatched pixels being those extracted from the plane A. The result of this checkerboard interlacing of the pixels is that the half tone created by the effect of the mean (a+b)/2="1/2" produces no flicker (column 3, lines 53-59).

In response to applicant's argument that claims 2 and 7 recite "the value of said first predetermined amount is selected as a function of said first pixel value." This argument is not persuasive because Barbier et al's teach the function value luminance of pixel a+ and a- in frame rate control (see figure 12A and 12B).

In response to applicant's argument that claims 3 and 8 recite "said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed." This argument is not persuasive because Barbier et al's teach the luminance level of a lit pixel "[+/-] a" = [+/-] 2 (for example) corresponds to the offsetting value as claimed; for example, a first offset pixel value a_{RGB} =14 and a second offset pixel value b_{RGB} = 18; based on the teaching of Barbier et al, the four luminance levels a+, a-, b+, b- are averaged during the periods 4/Fo; therefore, [+/-] 16 = (14+18) / 2 (see figures 7 and 8, column 5, lines 43-44);

In response to applicant's argument that claims 4 and 9 recite "said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame." This argument is not persuasive because Barbier et al's teach a graphic processor 2 offsets inherently a first pixel value close to a first bit a_{jk} and a second bit b_{jk} (a bit transition, column 3, lines 11-14) by the luminance level of a lit pixel "[+/-] a" = [+/-] 2 (for example) corresponds to the offsetting value as claimed, a first offset pixel value a_{RGB} =14 and a second offset pixel value b_{RGB} = 18 during a first display frame and a second display frame as claimed (see figures 7 and 8).

For these reasons, the rejections based on Barbier et al have been maintained.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kevin M. Nguyen** whose telephone number is **703-305-6209**. The examiner can normally be reached on MON-THU from 9:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reached on **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Kevin M. Nguyen
Examiner
Art Unit 2674

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600